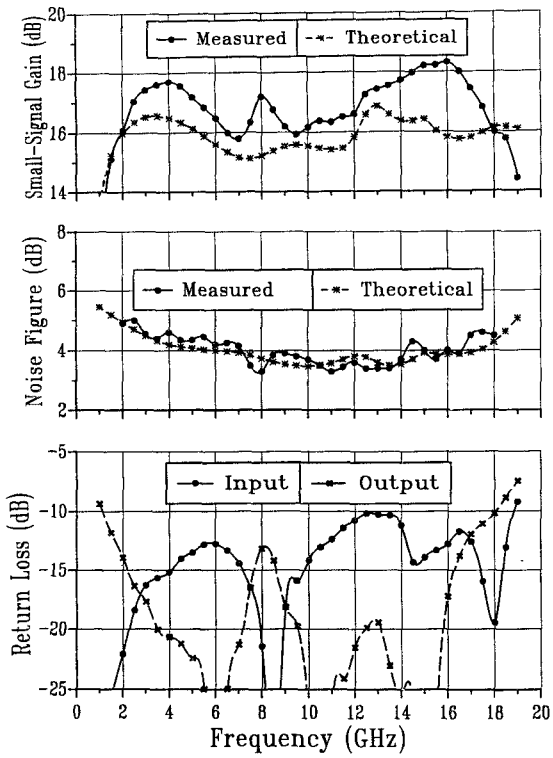

Fig. 8 Computed and experimental performance of the low-noise/high-gain module.

IV. Conclusion

An effort to develop monolithic 2–18 GHz matrix amplifiers has resulted in the successful fabrication of a high-gain/low-*VSWR* and a high-gain/low-noise module across the 2–18 GHz frequency band. The experimental results achieved represent the highest gains and lowest noise figures reported to date in monolithic 2–18 GHz amplifier modules using MESFET's.

Acknowledgment

The authors would like to thank S. M. Stulz, in whose section the wafers were fabricated, and R. D. Remba, in whose section the active devices were developed. Thanks go also to J. Martin, who assembled the amplifier modules, and S. J. Oberg, who developed the process for laser drilling the via holes.

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Monolithic GaAs p-i-n Diode Switch Circuits for High-Power Millimeter-Wave Applications

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***Abstract*—Two different *Ka*-band SPDT switch circuits using monolithic GaAs epitaxial p-i-n diode technology are presented. The lowest insertion loss is 0.7 dB at 35 GHz, and isolation is better than 32 dB from 30 to 40 GHz. The power handling capability is at least +38 dBm pulsed and +35 dBm CW. Switching speed rise and fall times are 2 ns.**

I. Introduction

The degree to which a millimeter-wave radar system can accurately locate a moving object is, in large part, dependent upon the RF transceiver section of the system. The transceiver performs the important function of interfacing computer processing and control with the transmitted and reflected radar signals. One of the more fundamental functions of a transceiver is to route signals from the antenna to the transmitter or receiver. The RF switch employed for this purpose should have low insertion loss and high power handling capabilities. A low-loss, high-power switch in the RF transceiver section is essential in realizing the full potential of a millimeter-wave system.

In this paper we describe the development and testing of monolithic SPDT switches designed to meet the progressively increasing power requirements of developing millimeter-wave systems. Previous work has been reported on monolithic switch circuits employing planar p-i-n structures [1], [2] or MESFET devices [3]. The switches presented here employ epitaxial vertical p-i-n diode structures [4] in a shunt configuration optimized for low loss and high isolation under high-power signal conditions. The vertical epitaxial structure is expected to provide lower RF impedance under forward bias than planar ion-implanted p-i-n structures [5] and to have power handling capability superior to that of MESFET's. An additional feature of the circuits described here is the location of the p-i-n diode directly underneath the RF line. This can improve isolation and increase bandwidth compared to planar devices, which are typically positioned adjacent to, or a quarter-wave from, the RF line.

II. Circuit Description

Fig. 1 illustrates the two SPDT designs investigated in this work. Each output arm contains a p-i-n diode spaced a quarter-wavelength from the common input arm. When forward biased, the low-impedance p-i-n diode is transformed through the quarter-wave section to present a high impedance at the switch junction. Simultaneously, the junction capacitance of the reverse-biased p-i-n in the second arm is tuned to a low-pass filter response by the inductive air bridge interconnects. In Fig. 1(a) via holes are used to ground the diodes while the design in Fig. 1(b) uses radial stubs to provide the RF ground at the diodes.

Insertion losses associated with the prototype design can be optimized by properly selecting the elements for a low ripple Chebyshev response. Analysis by computer predicts that most of the critical dimensions in the circuit depend upon the diode parameters. In order to reduce the amount of empirical work

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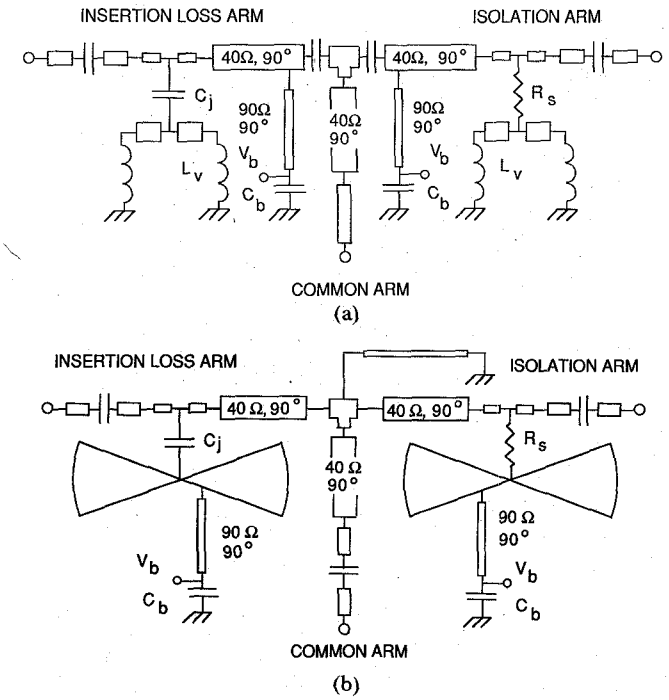


Fig. 1. Circuit models of prototype SPDT switch structures using (a) via holes and (b) radial stubs to ground the p-i-n diodes. Arm 1 is in the isolation state; arm 2 is in the loss state.

required to characterize the diode, a theoretical investigation was conducted to determine R_s and C_j as a function of the structure dimensions. The design curves generated from the computations were used in conjunction with computer analysis to identify possible diode structures that meet specified performance requirements. A simplified thermal analysis and voltage breakdown calculations were also included to ensure that the diodes selected would survive under high power conditions [6].

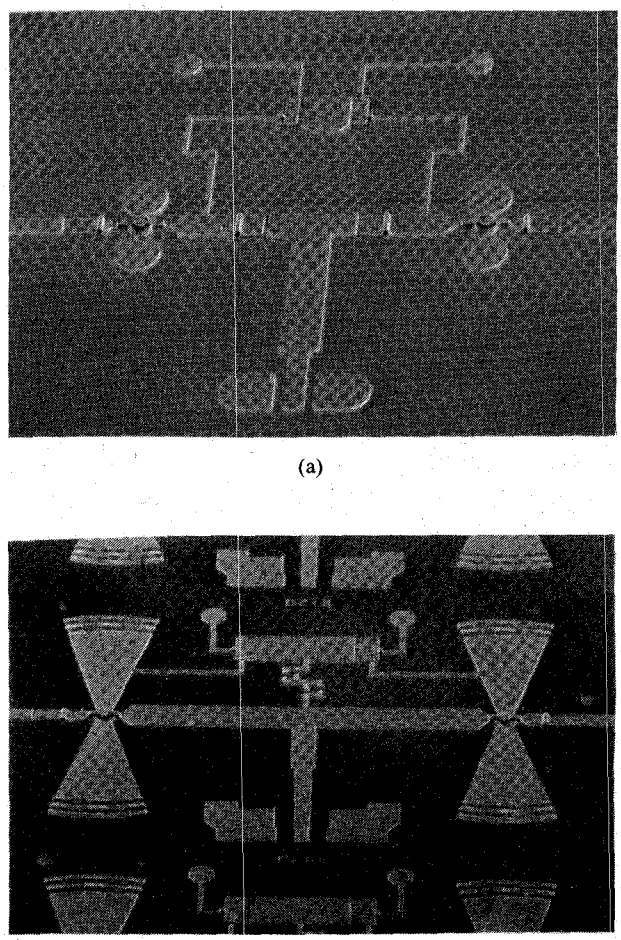
Photographs of the switches are shown in Fig. 2(a) and (b). Via holes are used to ground each diode in Fig. 2(a) and form coplanar probe pads at the RF input and output ports in both designs. Parasitic capacitances are minimized by chamfering the RF line near via holes. Bias is applied to the two pads near the top edge of the chip. The MIM capacitor, C_b, used in the bias filter conserves space and eliminates any bias port isolation problems that may occur with radial stubs. The chip measures 1.9×3.4 mm^2 (76×136 mils^2).

III. GaAs p-i-n Diode

A SEM photograph of the double mesa structure is shown in Fig. 3. The vertical epitaxial structure employed minimizes intrinsic resistance and increases carrier injection efficiency as compared to a planar structure [5]. The 50-μm-diameter diode shown here has a 0.4-μm-thick p^+ top layer with a free hole concentration of 2×10^{19} cm^{-3} followed by a 3-μm-thick intrinsic layer of 1×10^{15} cm^{-3} n-type material and a 4 μm, 2×10^{18} cm^{-3} n^+ bottom layer. The diode has a C_j of 65 fF at -5 V reverse bias and a R_s of 1.5 Ω at $+30$ mA forward bias.

IV. Fabrication

The p-i-n structures were grown by MOCVD on LEC semi-insulating GaAs substrates. Isotropic etching was used to fabricate the circular double mesa structure. Au/Ag/Zn and AuGe/Ni/Au evaporated films were alloyed into the p^+ and n^+ terminals respectively to form ohmic contacts. Evaporation and lift-off were used to defined transmission lines and dc bias pads. Diode passivation and dielectric layers for MIM capacitors were produced by PECVD of Si_3N_4 and plasma etching. Electroplating of transmission lines and air bridges completed front side wafer processing. After lapping and polishing the wafer to 100 μm, via holes were etched from the back side by reactive ion etching. Back-side metallization and plating provided the ground



(a)

(b)

Fig. 2. SEM photographs of the *Ka*-band switch with (a) via hole grounding and (b) raidal stub grounding.

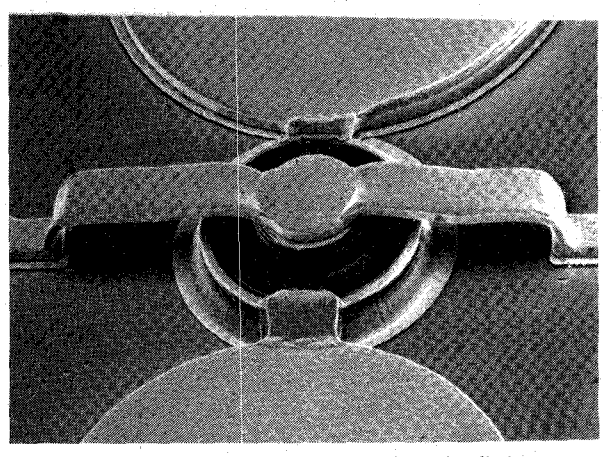


Fig. 3. SEM photograph of the vertical p-i-n diode.

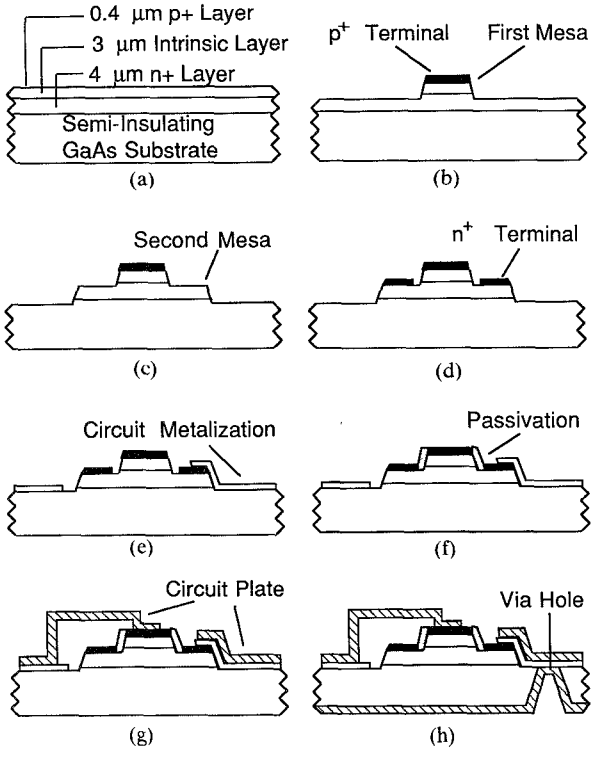


Fig. 4 Schematic diagram of MMIC switch processing: (a) GaAs substrate; (b) p+ contact metal alloy and first mesa etching; (c) second mesa etching; (d) n+ contact metal alloy; (e) circuit metallization; (f) passivation and MIM capacitor dielectric layer; (g) air bridge and circuit metal plating; (h) via hole etching and backside metallization.

plane. Street etching and chip separation completed the process. A schematic diagram of the fabrication steps is shown in Fig. 4.

V. Experimental Results

Wafer evaluation used a copolanar waveguide probe station and an automated vector network analyzer. Results for a via hole grounded design are shown in Fig. 5(a) and 5(c). Insertion loss is 0.7 dB at 35 GHz. Isolation is better than 32 dB from 30 to 40 GHz. The return loss of the common arm is better than 40 dB (1.05:1 *VSWR*) at 37.5 GHz, indicating that the quarter-wave sections should be reduced slightly to center the response at 35 GHz. Results for a radial stub grounded design are shown in Fig. 5(b) and (c). Insertion loss is 1.2 dB at 35 GHz. Isolation is a maximum at 34 GHz and follows the quarter-wave response of the radial stubs over the band. The relatively flat return loss indicates that circuit parameters need to be adjusted to fully tune the switch structure.

Switches with via hole grounds were used to evaluate high power handling capabilities. Fig. 6 is a photograph of the test fixture used for high power testing. The quartz microstrip boards that interconnect the chip with the coax-to-microstrip transitions are recessed in channels to enhance arm-to-arm isolation. Bias pins can be seen at the front of the fixture. The fixture has 1.1 dB loss and 22 dB of return loss at the test frequency of 35 GHz.

The essential details of the high power measurement system are illustrated in Fig. 7. A pulsed IMPATT source supplied +38 dBm to the device under test with a pulse width of roughly 100 ns. A sweep generator and TWT amplifier provided +35 dBm for the CW test. These power levels were the maximum possible with the available test equipment. Insertion loss and isolation were monitored using power meters. Bias for the arm in isolation

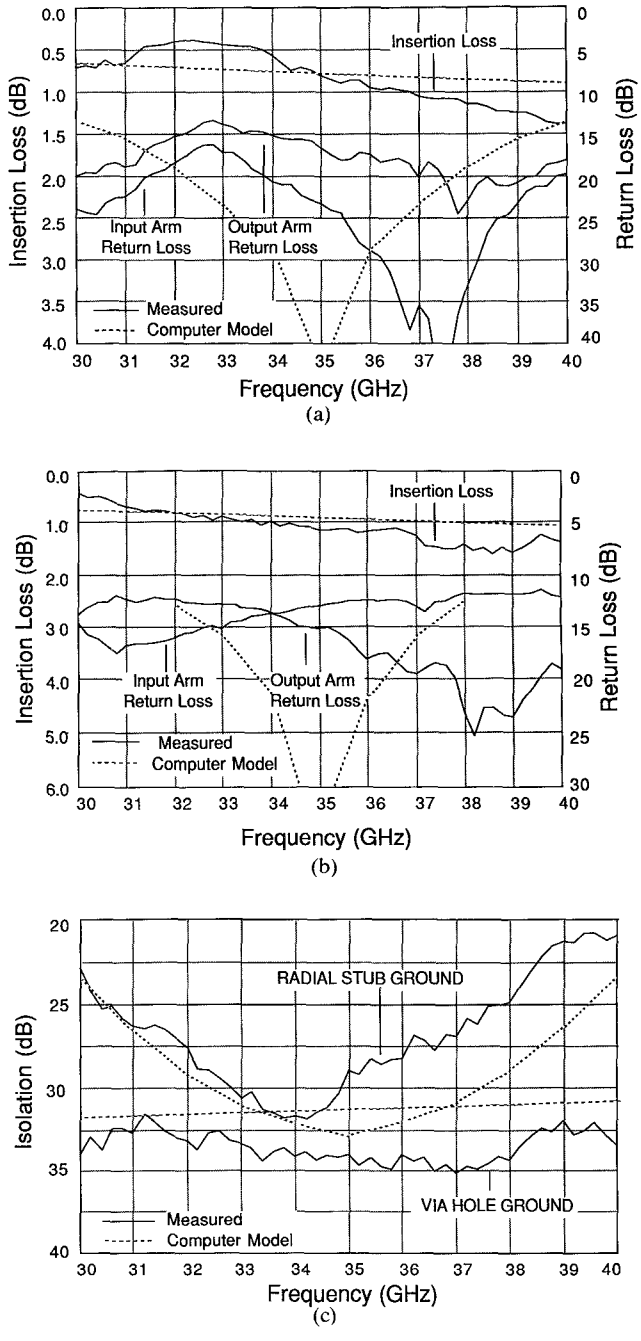


Fig. 5. Insertion loss characteristics of (a) the via hole ground SPDT switch (diode diameter: 50 μm; I-layer thickness: 3 μm), (b) the radial stub grounded SPDT switch (diode diameter 42 μm, I-layer thickness: 4 μm), and (c) isolation characteristics of the SPDT switches. Bias: loss arms; −5 Vdc, isolation arms. 15 mA.

was held at +25 mA during the 40 minute testing intervals. Initially the bias for the low-loss arm was set to −5 V. However the bias level had to be increased to more than −15 V during high power testing to maintain minimum insertion loss. The increased bias level was necessary to prevent charge injected into the I region during forward-going RF voltage excursions from multiplicatively increasing through impact ionization with each succeeding RF cycle [6]. Degradation in performance was not observed after the bias level was adjusted and the results of a small-signal RF evaluation were identical, within experimental error, to previously recorded data.

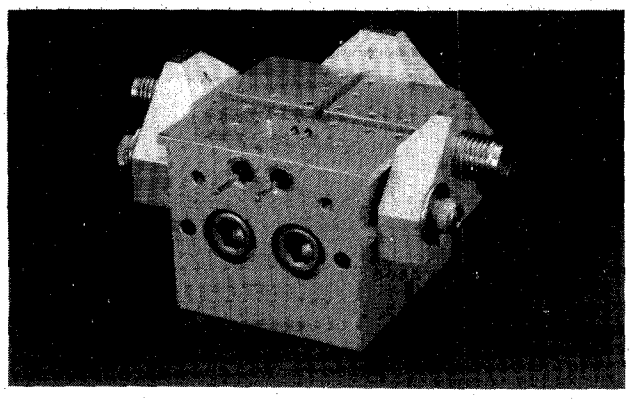


Fig. 6. Microstrip test fixture for high power testing.

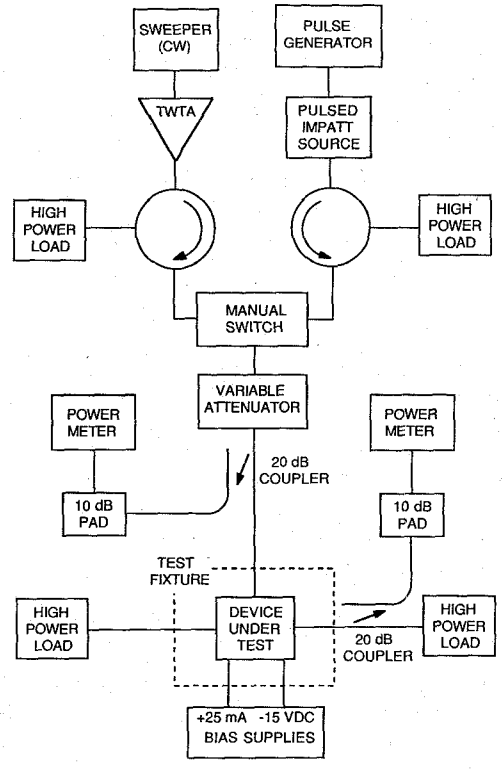


Fig. 7. High power test stand block diagram.

Switching speed measurements were performed on the design with via hole grounds. The 10 to 90 percent RF and 90 to 10 percent RF rise and fall times are 2 ns. The 50 percent TTL to 90 percent RF and 50 percent TTL to 10 percent RF times are 10 ns. The Alpha 66245 inverting driver that applied +10 mA and −12 V to the switch has a 7 ns delay between the 50 percent TTL and 50 percent output drive levels. Photographs of the measurement are given in [7].

VI. Conclusion

The monolithic *Ka*-band p-i-n diode switches described here have demonstrated excellent millimeter-wave characteristics under high power conditions. The radial stub grounded design does not match the broad-band performance of the via hole design, but the elimination of back-side wafer processing simplifies fabrication. Insertion loss for the via hole grounded design is 0.7 dB at 35 GHz and isolation is better than 32 dB from 30 to 40 GHz. The switch is capable of handling +38 dBm pulsed and +35 dBm CW, which were the maximum power ratings of the test equipment available. Switching speed is 2 ns.

Acknowledgment

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Ka-Band MMIC Beam-Steered Transmitter Array

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***Abstract*—A 32 GHz six-element linear transmitter array utilizing MMIC phase shifters and power amplifiers has been designed and tested as part of the development of a spacecraft array feed for NASA deep-space communications applications. Measurements of the performance of individual phase shifters, power amplifiers, and microstrip radiators were carried out and electronic beam steering of the linear array was demonstrated.**

I. Introduction

Communication systems for NASA deep-space missions presently operate at *X*-band (8 GHz). However, in the mid-1990's, advanced deep-space missions will utilize *Ka*-band systems (32 GHz down-link, 34 GHz up-link) to achieve communications enhancement on the order of 8 dB. A receiver MMIC array at *Ka*-band has been reported [1], but a transmitter array, a critical element in these systems, has not.

At JPL a 32 GHz solid-state transmitter is under development utilizing state-of-the-art GaAs MMIC devices. The inital goal of this work is to produce a *Ka*-band planar phased array with 5 W output power to feed a 4 m reflector system. The electronic beam

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